

REMARKS

FIGURE 1. has been amended, new FIGURE 5 has been added, the specification has been amended, and claims 6, 7, 17, 19, and 20 have been amended.

Applicant respectfully requests further examination and reconsideration of claims 1-20, still pending in the application.

The first Office Action mailed from the Patent Office on February 9, 2004 has been carefully considered and indicates that:

- a) The drawings are objected to under 37 CFR § 1.83(a);
- b) The drawings are objected to under 37 CFR § 1.84(o);
- c) Claims 3 and 5-20 are rejected under 35 U.S.C. § 112, *second paragraph*, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention;
- d) Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kean et al.;
- e) Claims 5 and 8-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean et al. in view of "Digital systems Testing and Testable Design" Abramovici et al.; and
- f) Claims 6, 7, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean et al. in view of "Digital systems Testing and Testable Design" Abramovici et al. and further in view of Frisch et al.

In response to the Examiner's objection to the drawings under 37 CFR § 1.83(a), applicant has:

1. Added new FIGURE 5 (flow chart) to show every feature specified in claim 17, as required by the Examiner.
2. Replaced paragraphs [0016] and [0017] of the specification with "[0016] Figure 3 is a block diagram of an FPGA test circuit of an embodiment of the present invention; [0017] Figure 4 illustrates an FPGA coupled to a tester circuit; and".
3. Added "Figure 5 is a flow chart of the method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA)" directly after paragraph [0017] of the specification.
4. Added "Figure 5 is a flow chart of the method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA)" directly after paragraph [0028] of the specification.

In view of the amendments to the drawings and the specification noted in 1-4 above, applicant respectfully submits that the Examiner's grounds for the objection to the drawings under 37 CFR § 1.83(a) no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw this objection.

In response to the Examiner's objection to the drawings under 37 CFR § 1.84(o), applicant has amended FIGURE 1 to include descriptive labels in addition to the numeral labels already present, as required by the Examiner.

In view of the amendment made *supra* to FIGURE 1 to include descriptive labels in addition to the numeral labels already present, applicant respectfully submits that the Examiner's grounds for the objection to the drawings under 37 CFR § 1.84(o) no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw this objection.

In response to the Examiner's rejection of claims 3 and 5-20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, applicant:

1. Respectfully submits that there are two types of clock stresses: frequency offset; and phase noise (jitter). As serial receivers perform clock recovery, the clock is embedded in the transmitted data. One can change the transmit data rate by +/- 100 parts per million in frequency (typical specification) to stress the receiver. One can also add phase noise, or jitter the transmit clock to provide a stress to the receiver's clock recovery circuits.
2. Respectfully submits that since the clock is embedded in the data pattern, if one has no change in the data pattern, the clock information is eventually lost by too many consecutive 1's or 0's. Stress patterns then consist of varying amounts of long runs of 1's and 0's alternated with other patterns, which are changed at a regular interval, which have the effect of creating phase noise or jitter in the receiver's clock recovery circuits. This stresses the receiver. A good receiver will tolerate a given amount of stress, whereas a bad receiver will not.
3. Has amended steps 3 and 4 of claim 17 to insert --circuit-- after "SERDES", amended step 2 of claim 19 to insert --circuit-- after "SERDES", and amended step 2 of claim 20 to insert --circuit-- after "SERDES", so as to eliminate antecedent basis issues.
4. Has amended step 2 of claim 17 to delete "circuitry" before "array" and amended step 7 of claim 17 to insert --logic-- before "array", so as to eliminate antecedent

basis issues.

In view of the arguments presented *supra*, and the amendments to claims 17, 19 and 20 noted in 3-4 above, applicant respectfully submits that the Examiner's grounds for the rejection of claims 3 and 5-20 under 35 U.S.C. § 112, *second paragraph*, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw this rejection.

In response to the Examiner's rejection of claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Kean *et al.*, the Examiner's rejection of claims 5 and 8-19 under 35 U.S.C. § 103(a) as being unpatentable over Kean *et al.* in view of "Digital systems Testing and Testable Design" Abramovici *et al.*, and the Examiner's rejection of claims 6, 7, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Kean *et al.* in view of "Digital systems Testing and Testable Design" Abramovici *et al.* and further in view of Frisch *et al.*, applicant respectfully submits that:

1. Claim 1 discloses at least the following advantageous distinctive features that distinguish over and avoid the prior art:

- a) "a serializer/deserializer circuit coupled to the data communication connection and the logic array;"
and
- b) "the logic array is programmable to perform test operations on the serializer/deserializer circuit, and reprogrammed later to perform an end application."

2. Claim 5 discloses at least the following advantageous distinctive features that distinguish over and avoid the prior art:

- a) "a serializer/deserializer circuit coupled to the input and output data communication connections;"
- b) "a logic array programmed to generate a test data pattern coupled to the output data communication connection;" and
- c) "the logic array is further programmed to check a data pattern received on the input data communication connection..."

3. Claim 10 discloses at least the following advantageous distinctive features that distinguish over and avoid the prior art:

- a) "generating a test pattern using programmed logic circuitry of the FPGA;"
- b) "outputting the test pattern on an output connection;"
- c) "coupling the test pattern to an input connection of the high speed interconnect circuit;"
- d) "evaluating data received on the input connection using the programmed logic circuitry;" and
- e) "storing data indicating a result of the evaluation"

4. Claim 14 discloses at least the following advantageous distinctive features that distinguish over and avoid the prior art:

- a) "a test circuit;"

- b) "a field programmable gate array (FPGA) coupled to the test circuit;"
- c) "the FPGA comprises input and output data communication connections coupled together through the test circuit;"
- d) "the FPGA comprises a serializer/deserializer (SERDES) circuit coupled to the input and output data communication connections;"
- e) "the FPGA comprises a logic array programmed to generate a test data pattern coupled to the output data communication connection;" and
- f) "the logic array is further programmed to check a data pattern received on the input connection..."

5. Claim 17 discloses at least the following advantageous distinctive features that distinguish over and avoid the prior art:

- a) "programming a logic array of the FPGA";
- b) "generating a test pattern using the programmed logic array of the FPGA";
- c) "outputting the test pattern on an output connection of the SERDES circuit";
- d) "externally coupling the test pattern to an input connection of the SERDES circuit";
- e) "using the programmed logic array, evaluating data received on the input connection";

- f) "storing data indicating a result of the evaluation in a memory circuit of the FPGA"; and
- g) "re-programming the logic array to perform an end user application"

The advantages of these arrangements of claims 1, 5, and 14 discussed *supra* include:

1. By coupling the serdes to the user logic, the data may now be used for something other than configuration. This is a much broader use of the serdes, and may be used for telephony, data communications, data processing, and data switching applications.
2. By utilizing existing user programmable logic to perform test functions, that same logic may be reprogrammed by the customer to then provide the intended application/use with zero added cost.

The advantages of these arrangements of claims 10 and 17 discussed *supra* include by utilizing existing user programmable logic to perform test functions, not only can that same logic be reprogrammed by the customer to then provide the intended application/use with zero added cost, but it is also able to provide stress patterns through the use of varying the data patterns in the user logic.

Turning now to the references, in contradistinction, Kean et al. do not teach advantageous distinctive feature a) of claim 1 and advantageous distinctive feature a) of claim 10 discussed *supra*. Instead, Kean et al. teach that the serializer/deserializer is not connected to the logic fabric for use by the user's logic or design, but rather is connected to the configuration circuits for the purpose of providing data to the memory cells for configuration purposes. Additionally, the serializer/deserializer of Kean et al. does not perform clock

recovery, and uses two pins, one for data, and one for clock, as opposed to one pin for data that includes the embedded clock information. There are connections from the user array to the configuration logic so that the user can access the configuration for self program or self test, but not so that the user can access the serdes from the pins to the logic.

The disadvantage of this arrangement of Kean *et al.* is that the data can only be used for configuration.

Hence Kean *et al.* neither disclose nor teach advantageous distinctive feature a) of claim 1 and advantageous distinctive feature a) of claim 10, and for at least this reason alone, claims 1 and 10 should be allowable.

In further contradistinction, Kean *et al.* do not teach advantageous distinctive feature b) of claim 1, advantageous distinctive features b), c), and d) of claim 10, advantageous distinctive features a), b), c), e), and f) of claim 14, and advantageous distinctive features a), b), c), d), e), f), and g) of claim 17 discussed *supra*. Instead, Kean *et al.* teach a simple loop back test of clock and data for a functional test of the serializer/deserializer. For a multi-gigabit transceiver with embedded clock recovery, the loop back and the subsequent test strategy must be greatly expanded.

The disadvantage of this arrangement of Kean *et al.* is that the same logic cannot be reprogrammed by the customer to provide the intended application/use with zero added cost.

Hence Kean *et al.* neither disclose nor teach advantageous distinctive feature b) of claim 1, advantageous distinctive features b), c), and d) of claim 10, advantageous distinctive features a), b), c), e), and f) of claim 14, and advantageous distinctive features a), b), c), d), e), f), and g) of claim 17, and for at least this reason alone, claims 1, 10, 14, and 17 should be allowable.

In further contradistinction, Kean et al. do not teach advantageous distinctive feature a) of claim 5 and advantageous distinctive feature d) of claim 14 discussed *supra*, but rather teach a means for separating address and data from the serdes, as opposed to a general purpose serdes which has no dedicated structure for the data.

The disadvantage of this arrangement of Kean et al. is that the serdes is designed for one use, and cannot be used for customer applications.

Hence Kean et al. neither disclose nor teach advantageous distinctive feature a) of claim 5 and advantageous distinctive feature d) of claim 14, and for at least this reason alone, claims 5 and 14 should be allowable.

In further contradistinction, Kean et al. do not teach advantageous distinctive features b) and c) of claim 5 discussed *supra*, but rather teach dedicated interfaces that are not in user logic nor user accessible.

The disadvantage of this arrangement of Kean et al. is that the data can only be used for configuration.

Hence Kean et al. neither disclose nor teach advantageous distinctive features b) and c) of claim 5, and for at least this reason alone, claim 5 should be allowable.

In further contradistinction, Kean et al. do not teach advantageous distinctive feature e) of claim 10 discussed *supra*, but rather teach a simple loop back test of clock and data for a functional test of the serializer/deserializer. For a multi-gigabit transceiver with embedded clock recovery, the loop back and the subsequent test strategy must be greatly expanded. Basically, a simple functional loop back of this specialized configuration interface is totally insufficient to test a multi gigabit transceiver with integrated clock recovery as coupled to the user logic.

The disadvantage of this arrangement of Kean *et al.* is that the same logic cannot be reprogrammed by the customer to provide the intended application/use with zero added cost.

Hence Kean *et al.* neither disclose nor teach advantageous distinctive feature e) of claim 10, and for at least this reason alone, claim 10 should be allowable.

Regarding the Examiner's statement that "...it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the testing system of Abramovici *et al.* with the FPGA system of Kean *et al.*," there is no motivating suggestion either in the references themselves or in the knowledge of one skilled in the art provided by the Examiner to modify the FPGA of Kean *et al.* to use the testing system of Abramovici *et al.* The Examiner has merely combined elements in a piecemeal manner in light of applicant's disclosure to show obviousness by using applicant's own disclosure as though it were prior art, and in so doing, has violated the basic mandate of 35 U.S.C. § 103 that a piecemeal reconstruction of the prior art patents in light of applicant's disclosure shall not be the basis for a holding of obviousness.

Applicant respectfully submits that since claims 2-4 depend from claim 1, claims 2-4 should be allowable for at least the same reasons claim 1 is allowable.

Applicant respectfully submits that since claims 6-9 depend from claim 5, claims 6-9 should be allowable for at least the same reasons claim 5 is allowable.

Applicant respectfully submits that since claims 11-13 ultimately depend from claim 10, claims 11-13 should be allowable for at least the same reasons claim 10 is allowable.

Applicant respectfully submits that since claims 15 and 16 ultimately depend from claim 14, claims 15 and 16 should be allowable for at least the same reasons claim 14 is allowable.

Applicant respectfully submits that since claims 18-20 depend from claim 17, claims 18-20 should be allowable for at least the same reasons claim 17 is allowable.

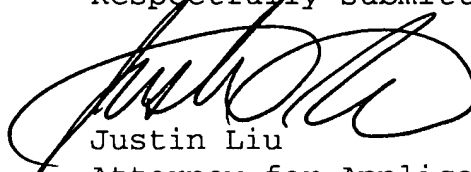
In view of the arguments presented *supra*, applicant respectfully submits that the Examiner's grounds for the rejection of claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Kean *et al.*, the Examiner's grounds for the rejection of claims 5 and 8-19 under 35 U.S.C. § 103(a) as being unpatentable over Kean *et al.* in view of "Digital systems Testing and Testable Design" Abramovici *et al.*, and the Examiner's grounds for the rejection of claims 6, 7, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Kean *et al.* in view of "Digital systems Testing and Testable Design" Abramovici *et al.* and further in view of Frisch *et al.* no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw this rejection.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-4641 (Pacific Standard Time).

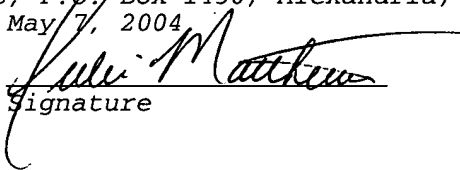
Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 7, 2004

Julie Matthews
Name



Signature